

Instruction Execution Times

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Introduction

This appendix contains several tables that provide the instruction execution times for DL105 Micro PLCs. Many of the execution times depend on the type of data used with the instruction. Registers may be classified into the following types:

- Data (word) Registers
- Bit Registers

V-Memory Data Registers

Some V-memory locations are considered data registers, such as timer or counter current values. Standard user V memory is classified as a V-memory data register. Note that you can load a bit pattern into these types of registers, even though their primary use is for data registers. The following locations are data registers:

Data Registers	DL105
Timer Current Values	V0 – V77
Counter Current Values	V1000 – V1077
User Data Words	V2000 – V2377 V4000 – V4177

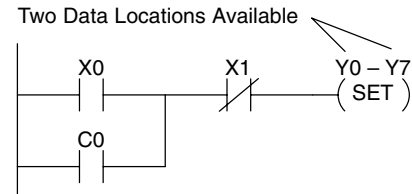
V-Memory Bit Registers

You may recall that some of the discrete points such as X, Y, C, etc. are automatically mapped into V memory (see Appendix E). The following bit registers contain this data:

Bit Registers	DL105
Input Points (X)	V40400 – V 40407
Output Points (Y)	V40500 – V40507
Control Relays (C)	V40600 – V40617
Timer Status Bits	V41100 – V41103
Counter Status Bits	V41140 – V41143
Stages	V41000 – V41017

How to Read the Tables

Some instructions can have more than one parameter. For example, the SET instruction shown in the ladder program to the right can set a single point or a range of points.



In these cases, execution times that depend on the amount and type of parameters. The execution time tables list execution times for both situations, as shown below:

SET	1st #: X, Y, C, S	17.4 μs
	2nd #: X, Y, C, S, (N pt)	12.0μs+5.4μs×N
RST	1st #: X, Y, C, S	19.5 μs
	2nd #: X, Y, C, S, (N pt)	10.5μs+5.2μs×N

Execution depends on numbers of locations and types of data used

Instruction Execution Times

Boolean Instructions

Boolean Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
STR	X, Y, C, T, CT, S, SP	3.3 μs	3.3 μs
STRN	X, Y, C, T, CT, S, SP	3.9 μs	3.9 μs
OR	X, Y, C, T, CT, S, SP	2.7 μs	2.7 μs
ORN	X, Y, C, T, CT, S, SP	3.3 μs	3.3 μs
AND	X, Y, C, T, CT, S, SP	2.1 μs	2.1 μs
ANDN	X, Y, C, T, CT, S, SP	2.7 μs	2.7 μs
ANDSTR	None	1.2 μs	1.2 μs
ORSTR	None	1.2 μs	1.2 μs
OUT	X, Y, C	3.4 μs	3.4 μs
OROUT	X, Y, C	8.6 μs	8.6 μs
PD	X, Y, C	13.5 μs	13.5 μs
SET	1st #: X, Y, C, S 2nd #: X, Y, C, S (N pt)	17.4 μs 12.0μs+5.4μsxN	6.8 μs 6.8 μs
RST	1st #: T, CT 2nd #: T, CT (N pt)	31.6 μs 17μs+14.6μsxN	6.8 μs 6.8 μs
PAUSE	1wd: Y 2wd: Y (N points)	19.0 μs 15μs+4μs x N	19.0 μs 15μs+4μs x N
RST	1st #: X, Y, C, S 2nd #: X, Y, C, S (N pt)	17.7 μs 10.5μs+5.2μsxN	6.8 μs 6.8 μs

Comparative Boolean Instructions

Comparative Boolean Instructions		DL105		
Instruction	Legal Data Types	Execute	Not Execute	
STRE	1st	2nd		
	V: Data Reg.	V:Data Reg.	77 μs	13.8 μs
		V:Bit Reg.	158 μs	13.8 μs
		K:Constant	57 μs	13.8 μs
	V: Bit Reg.	V:Data Reg.	158 μs	13.8 μs
		V:Bit Reg.	240 μs	13.8 μs
		K:Constant	139 μs	13.8 μs
STRNE	1st	2nd		
	V: Data Reg.	V:Data Reg.	77 μs	13.8 μs
		V:Bit Reg.	158 μs	13.8 μs
		K:Constant	57 μs	13.8 μs
	V: Bit Reg.	V:Data Reg.	158 μs	13.8 μs
		V:Bit Reg.	240 μs	13.8 μs
		K:Constant	139 μs	13.8 μs

Comparative Boolean (cont.)			DL105	
Instruction	Legal Data Types		Execute	Not Execute
ORE	1st	2nd		
	V: Data Reg.	V:Data Reg.	75 μs	12.0 μs
		V:Bit Reg.	158 μs	12.0 μs
		K:Constant	55 μs	12.0 μs
	V: Bit Reg.	V:Data Reg.	158 μs	12.0 μs
		V:Bit Reg.	239 μs	12.0 μs
		K:Constant	137 μs	12.0 μs
ORNE	1st	2nd		
	V: Data Reg.	V:Data Reg.	75 μs	12.0 μs
		V:Bit Reg.	158 μs	12.0 μs
		K:Constant	55 μs	12.0 μs
	V: Bit Reg.	V:Data Reg.	158 μs	12.0 μs
		V:Bit Reg.	239 μs	12.0 μs
		K:Constant	137 μs	12.0 μs
ANDE	1st	2nd		
	V: Data Reg.	V:Data Reg.	75 μs	12.0 μs
		V:Bit Reg.	158 μs	12.0 μs
		K:Constant	55 μs	12.0 μs
	V: Bit Reg.	V:Data Reg.	158 μs	12.0 μs
		V:Bit Reg.	239 μs	12.0 μs
		K:Constant	137 μs	12.0 μs
ANDNE	1st	2nd		
	V: Data Reg.	V:Data Reg.	75 μs	12.0 μs
		V:Bit Reg.	158 μs	12.0 μs
		K:Constant	55 μs	12.0 μs
	V: Bit Reg.	V:Data Reg.	158 μs	12.0 μs
		V:Bit Reg.	239 μs	12.0 μs
		K:Constant	137 μs	12.0 μs
STR	1st	2nd		
	T, CT	V:Data Reg.	78 μs	13.8 μs
		V:Bit Reg.	158 μs	13.8 μs
		K:Constant	57 μs	13.8 μs
	1st	2nd		
	V: Data Reg.	V:Data Reg.	78 μs	13.8 μs
	V:Bit Reg.	159 μs	13.8 μs	
	K:Constant	57 μs	13.8 μs	
V: Bit Reg.	V:Data Reg.	159 μs	13.8 μs	
	V:Bit Reg.	241 μs	13.8 μs	
		K:Constant	139 μs	13.8 μs
STRN	1st	2nd		
	T, CT	V:Data Reg.	78 μs	13.8 μs
		V:Bit Reg.	158 μs	13.8 μs
		K:Constant	57 μs	13.8 μs
	1st	2nd		
	V: Data Reg.	V:Data Reg.	78 μs	13.8 μs
	V:Bit Reg.	159 μs	13.8 μs	
	K:Constant	57 μs	13.8 μs	
V: Bit Reg.	V:Data Reg.	159 μs	13.8 μs	
	V:Bit Reg.	241 μs	13.8 μs	
		K:Constant	139 μs	13.8 μs

Comparative Boolean (cont.)			DL105	
Instruction	Legal Data Types		Execute	Not Execute
OR	1st T, CT	2nd V:Data Reg.	75 µs	12.0 µs
		V:Bit Reg.	158 µs	12.0 µs
		K:Constant	55 µs	12.0 µs
	1st V: Data Reg.	2nd V:Data Reg.	75 µs	12.0 µs
		V:Bit Reg.	158 µs	12.0 µs
		K:Constant	55 µs	12.0 µs
V: Bit Reg.	V:Data Reg.	158 µs	12.0 µs	
	V:Bit Reg.	240 µs	12.0 µs	
	K:Constant	137 µs	12.0 µs	
ORN	1st T, CT	2nd V:Data Reg.	75 µs	12.0 µs
		V:Bit Reg.	158 µs	12.0 µs
		K:Constant	55 µs	12.0 µs
	1st V: Data Reg.	2nd V:Data Reg.	75 µs	12.0 µs
		V:Bit Reg.	158 µs	12.0 µs
		K:Constant	55 µs	12.0 µs
V: Bit Reg.	V:Data Reg.	158 µs	12.0 µs	
	V:Bit Reg.	240 µs	12.0 µs	
	K:Constant	137 µs	12.0 µs	
AND	1st T, CT	2nd V:Data Reg.	76 µs	12.0 µs
		V:Bit Reg.	158 µs	12.0 µs
		K:Constant	55 µs	12.0 µs
	1st V: Data Reg.	2nd V:Data Reg.	75 µs	12.0 µs
		V:Bit Reg.	158 µs	12.0 µs
		K:Constant	55 µs	12.0 µs
V: Bit Reg.	V:Data Reg.	158 µs	12.0 µs	
	V:Bit Reg.	240 µs	12.0 µs	
	K:Constant	137 µs	12.0 µs	
ANDN	1st T, CT	2nd V:Data Reg.	76 µs	12.0 µs
		V:Bit Reg.	158 µs	12.0 µs
		K:Constant	55 µs	12.0 µs
	1st V: Data Reg.	2nd V:Data Reg.	76 µs	12.0 µs
		V:Bit Reg.	158 µs	12.0 µs
		K:Constant	55 µs	12.0 µs
V: Bit Reg.	V:Data Reg.	158 µs	12.0 µs	
	V:Bit Reg.	240 µs	12.0 µs	
	K:Constant	137 µs	12.0 µs	

Immediate Instructions

Immediate Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
STRI	X	27 μs	9.8 μs
STRNI	X	26 μs	8.6 μs
ORI	X	27 μs	9.8 μs
ORNI	X	26 μs	8.6 μs
ANDI	X	25 μs	8.0 μs
ANDNI	X	24 μs	6.8 μs
OROUTI	Y	45 μs	45 μs
SETI	1st #: Y	25.5 μs	6.8 μs
	2nd #: Y (N pt)	5.5 μs+20 x N	6.8 μs
RSTI	1st #: Y	25.5 μs	6.8 μs
	2nd #: Y (N pt)	5 μs+20.5 x N	6.8 μs

Timer, Counter, Shift Register, EDRUM Instructions

Timer, Counter, Shift Register, and Drum Instructions			DL105	
Instruction	Legal Data Types		Execute	Not Execute
TMR	1st	2nd		
	T	V:Data Reg.	75 μs	31 μs
		V:Bit Reg.	158 μs	31 μs
		K:Constant	66 μs	31 μs
TMRF	1st	2nd		
	T	V:Data Reg.	75 μs	31 μs
		V:Bit Reg.	158 μs	31 μs
		K:Constant	66 μs	31 μs
TMRA	1st	2nd		
	T	V:Data Reg.	94 μs	56 μs
		V:Bit Reg.	304 μs	264 μs
		K:Constant	95 μs	45 μs
TMRAF	1st	2nd		
	T	V:Data Reg.	98 μs	54 μs
		V:Bit Reg.	304 μs	264 μs
		K:Constant	95 μs	49 μs
CNT	1st	2nd		
	CT	V:Data Reg.	68 μs	61 μs
		V:Bit Reg.	148 μs	141 μs
		K:Constant	56 μs	45 μs
SGCNT	1st	2nd		
	CT	V:Data Reg.	57 μs	64 μs
		V:Bit Reg.	140 μs	148 μs
		K:Constant	46 μs	53 μs

Timer, Counter, Shift Register, and Drum Instructions Cont'd		DL105	
Instruction	Legal Data Types	Execute	Not Execute
UDC	1st		
	2nd		
	CT	V:Data Reg. V:Bit Reg. K:Constant	103 μs 310 μs 102 μs
SR	C (N points to shift)	30 μs+4.6 μs xN	17.2 μs
EDRUM	CT	320 μs	221 μs

Accumulator Data Instructions

Accumulator / Stack Load and Output Data Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
LD	V:Data Reg.	68 μs	8.4 μs
	V:Bit Reg.	149 μs	8.4 μs
	K:Constant	62 μs	8.4 μs
	P:Indir. (Data)	169 μs	8.4 μs
	P:Indir. (Bit)	256 μs	8.4 μs
LDD	V:Data Reg.	72 μs	8.4 μs
	V:Bit Reg.	266 μs	8.4 μs
	K:Constant	64 μs	8.4 μs
	P:Indir. (Data)	172 μs	8.4 μs
	P:Indir. (Bit)	373 μs	8.4 μs
LDF	1st		
	2nd		
	X, Y, C, S T, CT, SP	K:Constant (N pt)	77 μs+6.2 μs xN 10 μs
LDA	O: (Octal constant for address)	58 μs	8.4 μs
OUT	V:Data Reg.	60 μs	8.4 μs
	V:Bit Reg.	132 μs	8.4 μs
	P:Indir. (Data)	162 μs	8.4 μs
	P:Indir. (Bit)	239 μs	8.4 μs
OUTD	V:Data Reg.	68 μs	8.4 μs
	V:Bit Reg.	276 μs	8.4 μs
	P:Indir. (Data)	196 μs	8.4 μs
	P:Indir. (Bit)	384 μs	8.4 μs
OUTF	1st		
	2nd		
	X, Y, C	K:Constant (N pt)	36 μs+7.6 μs xN 8 μs
POP	None	55 μs	7.2 μs

Logical Instructions

Logical (Accumulator) Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
AND	V:Data Reg. V:Bit Reg.	63 μ s 261 μ s	10.4 μ s 10.4 μ s
ANDD	K:Constant	53 μ s	8.4 μ s
OR	V:Data Reg. V:Bit Reg.	59 μ s 257 μ s	10.4 μ s 10.4 μ s
ORD	K:Constant	49 μ s	8.4 μ s
XOR	V:Data Reg. V:Bit Reg.	60 μ s 257 μ s	10.4 μ s 10.4 μ s
XORD	K:Constant	49 μ s	8.4 μ s
CMP	V:Data Reg. V:Bit Reg.	59 μ s 259 μ s	10.4 μ s 10.4 μ s
CMPD	V:Data Reg. V:Bit Reg. K:Constant	63 μ s 257 μ s 54 μ s	8.4 μ s 8.4 μ s 8.4 μ s

Math Instructions

Math Instructions (Accumulator)		DL105	
Instruction	Legal Data Types	Execute	Not Execute
ADD	V:Data Reg. V:Bit Reg.	198 μ s 397 μ s	10.6 μ s 10.6 μ s
ADDD	V:Data Reg. V:Bit Reg. K:Constant	198 μ s 397 μ s 188 μ s	8.4 μ s 8.4 μ s 8.4 μ s
SUB	V:Data Reg. V:Bit Reg.	200 μ s 397 μ s	10.6 μ s 10.6 μ s
SUBD	V:Data Reg. V:Bit Reg. K:Constant	198 μ s 392 μ s 190 μ s	8.4 μ s 8.4 μ s 8.4 μ s
MUL	V:Data Reg. V:Bit Reg. K:Constant	497 μ s 483 μ s 487 μ s	10.6 μ s 10.6 μ s 8.4 μ s
DIV	V:Data Reg. V:Bit Reg. K:Constant	909 μ s 1108 μ s 899 μ s	10.6 μ s 10.6 μ s 8.4 μ s
INCB	V:Data Reg. V:Bit Reg.	83 μ s 349 μ s	10.4 μ s 10.4 μ s
DECB	V:Data Reg. V:Bit Reg.	82 μ s 351 μ s	10.4 μ s 10.4 μ s

Bit Instructions

Bit Instructions (Accumulator)		DL105	
Instruction	Legal Data Types	Execute	Not Execute
SHFR	V:Data Reg. (N bits)	44 μ s+14.6 x N	10.4 μ s
	V:Bit Reg. (N bits)	243 μ s+14.6 x N	10.4 μ s
	K:Constant (N bits)	34 μ s+14.6 x N	8.4 μ s
SHFL	V:Data Reg. (N bits)	44 μ s+14.6 x N	10.4 μ s
	V:Bit Reg. (N bits)	243 μ s+14.6 x N	10.4 μ s
	K:Constant (N bits)	34 μ s+14.6 x N	8.4 μ s
ENCO	None	62 μ s	7.2 μ s
DECO	None	34 μ s	7.2 μ s

Number Conversion Instructions

Number Conversion Instructions (Accumulator)		DL105	
Instruction	Legal Data Types	Execute	Not Execute
BIN	None	359 μ s	7.2 μ s
BCD	None	403 μ s	7.2 μ s
INV	None	27 μ s	5.0 μ s

Table Instructions

Table Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
MOV	Move V:data reg. to V:data reg.	450 μ s+17 x N	6.2 μ s
	Move V:bit reg. to V:data reg.	430 μ s+244 x N	6.2 μ s
	Move V:data reg to V:bit reg.	460 μ s+215 x N	6.2 μ s
	Move V:bit reg. to V:bit reg. N= #of words	490 μ s+448 x N	6.2 μ s
MOVMC	Move V:Data Reg. to E ²	—	—
	Move V:Bit Reg. to E ²	—	—
	Move from E ² to V:Data Reg.	250 μ s+201xN	6.2 μ s
	Move from E ² to V:Bit Reg. N= #of words	—	—
LDLBLE	K	58 μ s	8.4 μ s

CPU Control Instructions

CPU Control Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
NOP	None	0 μs	0 μs
END	None	27 μs	27 μs
STOP	None	16 μs	5 μs

Program Control Instructions

Program Control Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
MLS	K (1–7)	12 μs	12 μs
MLR	K (0–6) N= 1 to 7	13 μs + 2.4 x N	13 μs + 2.4 x N

Interrupt Instructions

Interrupt Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
ENI	None	9 μs	5 μs
DISI	None	8 μs	5 μs
INT	O0	0 μs	0 μs
IRT	None	1.6 μs	—

Message Instructions

Message Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
FAULT	V:Data Reg.	171 μs	8.4 μs
	V:Bit Reg.	253 μs	8.4 μs
	K:Constant	2798 μs	8.4 μs
DLBL	K	0 μs	0 μs
NCON	K	0 μs	0 μs
ACON	K	0 μs	0 μs

RLL^{PLUS} Instructions

RLL ^{PLUS} Instructions		DL105	
Instruction	Legal Data Types	Execute	Not Execute
ISG	S	31 μs	32 μs
SG	S	31 μs	32 μs
JMP	S	14 μs	8 μs